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(54) IMPROVEMENTS IN OR RELATING TO PHASE DETECTORS

(71) We, SIEMENS AKTIENGESELLSCHAFT, a German Company, of Berlin and Munich, Federal Republic of Germany, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to phase detectors, and more particularly to a phase detector for determining the phase difference between a binary measurement signal and a binary reference signal and for producing first and second pulsed output signals the pulse widths of the pulses of which depend upon the magnitude of the phase difference.

Phase detectors are frequently used in phase control circuits. The function of a phase control circuit is to produce a signal whose frequency and phase are controlled in such manner that the frequency is equal to the frequency of a reference signal and that a predetermined phase difference exists between the signal and the reference signal.

Normally a phase control circuit contains, in addition to a phase detector, a control device and a voltage-controlled oscillator. The voltage-controlled oscillator produces a signal having a controlled frequency and supplies this to the output of the phase control circuit and to an input of the phase detector as a measurement signal. A reference signal is applied to another input of the phase detector. The phase detector determines the phase difference between the measurement signal and the reference signal and feeds the control device with pulses whose widths depend upon the phase difference. The control device produces from these pulses a control voltage for the voltage-controlled oscillator which alters the frequency of the signal emitted by the latter in such a manner that any deviation from the given phase difference is counteracted.

Phase detectors are already known which determine the phase difference between a measurement signal and a reference signal. German Patent 1,801,261 describes a phase detector in which the reference signal is logic-linked to the measurment signal in a first AND-gate and is logic-linked to the inverted measurement signal in a second AND-gate. The outputs of the two AND-gates control current sources which emit positive or negative pulses of equal amplitude to an integrator element. The time integral of the pulses and thus the charge emitted by the current sources is, for phase differences of up to ± 90°, proportional to the phase difference between the measurement signal and the reference signal. This known phase detector determines the phase difference between the centres of the pulses of the reference signal and the rising or falling flanks of the pulses of the measurement signal.

This invention seeks to provide a phase detector which determines the phase difference between the rising flanks of a measurement and a reference signal for a phase difference range of ± 180°.

According to this invention there is provided a phase detector for determining the phase difference between a binary measurement signal and a binary reference signal and for producing first and second pulsed output signals the pulse widths of the pulses of which are dependent upon the magnitude of the phase difference, comprising a delay element which is arranged to delay the reference signal by a time which is equal to or greater than the period of the measurement signal and equal to, or less than, half the period of the reference signal, the period of the reference signal being equal to, or greated than, twice the period of the measurement signal, to produce a delayed reference signal, a bistable stage which is arranged to be set when the measurement signal, the reference signal, and the inverted delayed reference signal all have a first binary value and to be reset when the measurement signal has a second binary value and the delayed reference signal has the first binary value, a first logic element the output of which constitutes the first pulsed output signal and which emits a pulse when an output signal of the bistable stage, the inverted measurement signal, the reference signal, and the inverted delayed reference signal all have the first binary value, and a second logic element the output of which constitutes

the second pulsed output signal and which emits a pulse when the output signal of the bistable stage, the measurement signal, and the delayed reference signal all have the first binary value.

A phase detector in accordance with the invention has the advantage that it operates with great accuracy, in particular when very small phase differences exist. In this case narrow pulses do not have to be processed, but instead the relative time difference between pulses of different widths is formed. In addition the phase detector has the advantage that it does not emit pulses when reference signals are absent.

Preferably the bistable stage comprises a third logic element which is responsive to the measurement signal, the reference signal, and the delayed reference signal to produce a setting signal, a fourth logic element which is responsive to the measurement signal and the delayed reference signal to produce a resetting signal, and a bistable trigger circuit having a setting input to which the setting signal is applied, a trigger input to which the resetting signal is applied, and a data input to which the second binary value is applied.

The invention will be further understood from the following description by way of example of an embodiment thereof with reference to the accompanying drawings, in which:—

Figure 1 shows a block circuit diagram of a phase detector;

Figure 2 shows time diagrams of signals which occur at various points in operation of the phase detector of Figure 1;

Figure 3 shows a characteristic curve of the phase detector of Figure 1; and

Figure 4 shows a more detailed circuit diagram of the phase detector of Figure 1.

The phase detector shown in Figure 1 comprises a bistable stage K, a delay element V, and two logic elements G1 and G2. The bistable stage K contains a bistable trigger circuit F and two logic elements G3 and G4. The phase detector is supplied via a first input B with a rectangular reference signal *b* and via a second input M with a rectangular measurement signal *m* whose period *tm* is half the nominal period *tb* of the reference signal *b*.

At a first output C and a second output D the phase detector emits pulsed signals *c* and *d* respectively. The difference between the pulse widths of the signals *c* and *d* is a measure of the phase difference between the rising flanks of the reference signal *b* and those of the measurement signal *m*.

When the phase detector is used in a phase control circuit, the signals *c* and *d* are conducted for example to a control device which supplies a control voltage for a voltage-controlled oscillator. The voltage-controlled oscillator produces the measurement signal *m* which is conducted to the phase detector.

The measurement signal *m* is conducted to the logic elements G1 and G2 and in the bistable trigger stage K is conducted to the logic elements G3 and G4. The reference signal *b* is supplied to the delay element V and the logic elements G1 and G3. The delay element V delays the reference signal *b* by a length of time which is equal to, or up to approximately 10% greater than, the period *tm* of the measurement signal *m* and is equal to, or up to approximately 10% less than, half the period *tb* of the reference signal *b*, the period *tb* being equal to, or up to approximately 20% greater than, twice the period *tm*. A delayed reference signal *b*1 produced at the output of the delay element V is conducted to the logic elements G1 and G3 and also to the logic element G4.

Further details of the phase detector illustrated in Figure 1 will be described together with the signals represented in Figure 2.

Figure 2 shows signals which occur during operation of the phase detector shown in Figure 1. In Figure 2 time *t* is plotted in the abscissa direction and the amplitudes of the signals are represented in the ordinate direction. As the signals are all binary signals they can only assume the binary values 0 and 1.

The rectangular pulses of the measurement signal *m* represented in Figure 2 have a pulse width which is equal to half the period *tm*. The nominal period *tb* of the reference signal *b* is equal to double the period *tm* and the width of each pulse of the reference signal *b* is equal to half the nominal period *tb*, i.e. is equal to *tm*. It is assumed that between times *t*1 and *t*4 the period of the reference signal *b* is $\frac{1}{8}$ greater than the nominal period *tb* and thus the phase difference between the rising flanks of the reference signal *b* and those of the measurement signal *m* varies during this period. It is further assumed that after the time *t*4 the period of the reference signal *b* is constant and equal to the nominal period *tb*, but that between the time *t*4 and a time *t*5 a pulse of the reference signal *b* is absent. The delayed reference signal *b*1 is shown in Figure 2 to be delayed in relation to the reference signal *b* by the period *tm* of the measurement signal *m*.

At the time *t*1 the rising flanks of a pulse of the delayed reference signal *b*1 and a pulse of the measurement signal *m* occur simultaneously, so at this time no phase difference *p* exists between the two signals. At times *t*2 and *t*3 the measurement signal *m* leads and a positive phase difference *p* exists. from the time *t*4 onwards the measurement signal *m* lags and the phase difference *p* is negative.

In the bistable stage K the logic element

G3 logic-links the reference signal *b*, the delayed reference signal *b*1, and the measurement signal *m* in such manner that a signal *s* produced at its output has the binary value 1 whenever the reference signal *b* and the measurement signal *m* have the binary value 1 and the delayed reference signal *b*1 simultaneously has the binary value 0. This signal *s* is conducted as a setting signal to a setting input of the bistable trigger circuit F, which is set, so that a signal *a* produced at its output has the binary value 1, whenever the signal *s* assumes the binary value 1.

The logic element G4 links the delayed reference signal *b*1 and the measurement signal *m* in such manner that a signal *r* produced at its output has the binary value 0 whenever the measurement signal *m* and the delayed reference signal *b*1 simultaneously have the binary value 1. The signal *r* is conducted as a resetting signal to a trigger input of the bistable trigger circuit F. The binary value 0 is permanently supplied to an associated data input, and when the resetting signal *r* changes its binary value from 0 to 1 the binary value 0 is received by the bistable trigger circuit F which consequently is reset so that the signal *a* assumes the binary value 0.

The signal *a* is conducted to the logic elements G1 and G2. The logic element G1 logic-links the signal *a*, the measurement signal m, the reference signal *b*, and the delayed reference signal *b*1 in such manner that at the output C connected to the output of the element G1 the signal *c* has the binary value 1, i.e. a pulse of the signal *c* is produced, when the signal *a* and the reference signal *b* have the binary value 1 and at the same time the delayed reference signal *b*1 and the measurement signal *m* have the binary value 0. The logic element G2 logic-links the signal *a* with the measurement signal *m* and the delayed reference signal *b*1 in such manner that at the output D connected to the output of the element G2 the signal *d* has the binary value 1, i.e. a pulse of the signal *d* is produced, when the signal *a*, the measurement signal *m*, and the delayed reference signal *b*1 all simultaneously have the binary value 1.

At the time *t*1 no phase difference *p* exists between the measurement signal *m* and the delayed reference signal *b*1, so that the pulse of the signal *c* which is terminated at this time and the pulse of the signal *d* which commences at this time both have a width which is equal to the width of the rectangular pulses of the measurement signal *m*.

At the time *t*2 the measurement signal *m* leads the delayed reference signal *b*1 by 90° in relation to the period *tm*. The pulse width *tc* of the pulse of the signal *c* which is terminated at this time is again equal to the pulse width of the measurement signal *m*, but the pulse width *td* of the corresponding pulse of the signal *d* is now only half the width *tc*.

At the time *t*3 the measurement signal *m* leads by a phase difference *p* of 180°. The width of the pulse of the signal *c* is again equal to that of the pulses of the measurement signal *m*. The corresponding pulse of the signal *d*, on the other hand, now either no longer exists or, as shown in Figure 2, has a very small width.

From the time *t*4 onwards the measurement signal *m* lags by a constant phase difference of 90°. Consequently from this time onwards the width of each pulse of the signal *d* is equal to that of the pulses of the pulses of the measurement signal *m*, and each pulse of the signal *c* has only half this width.

As it has been assumed that a rectangular pulse of the reference signal *b* is absent between the times *t*4 and *t*5, no corresponding pulses of the signals *c* and *d* are then produced.

Figure 3 illustrates a characteristic curve of the phase detector. The phase difference *p* between the measurement signal *m* and the delayed reference signal *b*1 is plotted in the abscissa direction. This phase difference *p* is related to the period of the measurement signal *m*. The difference *tc* — *td* of the pulse widths *tc* and *td* is plotted in the ordinate direction. The characteristic curve has a saw-tooth shaped courses which is repeated with a period of 360°. It also shows that the phase detector possesses a linear course in a range between −180° and +180° of each period. The phase difference between the measurement signal *m* and the undelayed reference signal *b* can also be seen from the characteristic curve if the ordinate is displaced in the abscissa direction by the delay time, produced by the delay element V, related to the period of the measurement signal *m*. With the assumed delay time which is equal to the period *tm* of the measurement signal *n*, the ordinate is displaced to the left by a phase angle of 360°.

Figure 4 shows the phase detector in more detail. The delay element V is for example a transit time element or, if an appropriate pulse train signal exists, a shift register. The logic element G1 consists of an AND gate U1 and an inverter J1. The AND gate U1 is supplied with the measurement signal *m* inverted by the inverter J1, the reference signal *b*, the signal *a*, and the delayed reference signal *b*1 inverted by an inverter J2 in the logic element G3. The logic element G2 consists of an AND gate U2, which logic-links the measurement signal *m*, the delayed reference signal *b*1, and the signal *a*.

The logic element G3 consists of the inverter J2 and an AND gate U3. The AND

gate U3 logic-links the measurement signal *m*, the reference signal *b*, and the inverted reference signal *b*1, and produces the setting signal *s* at its output. The logic element G4 consists of a NAND gate N which logic-links the measurement signal *m* with the delayed reference signal *b*1 and produces the resetting signal *r* at its output.

WHAT WE CLAIM IS:—

1. A phase detector for determining the phase difference between a binary measurement signal and a binary reference signal and for producing first and second pulsed output signals the pulse widths of the pulses of which are dependent upon the magnitude of the phase difference, comprising a delay element which is arranged to delay the reference signal by a time which is equal to or greater than the period of the measurement signal and equal to, or less than, half the period of the reference signal, the period of the reference signal being equal to, or greater than, twice the period of measurement signal, to produce a delayed reference signal, a bistable stage which is arranged to be set when the measurement signal, the reference signal, and the inverted delayed reference signal all have a first binary value and to be reset when the measurement signal has a second binary value and the delayed reference signal has the first binary value, a first logic element the output of which constitutes the first pulsed output signal and which emits a pulse when an output signal of the bistable stage, the inverted measurement signal, the reference signal, and the inverted delayed reference signal all have the first binary value, and a second logic element the output of which constitutes the second pulsed output signal and which emits a pulse when the output signal of the bistable stage, the measurement signal, and the delayed reference signal all have the first binary value.

2. A phase detector as claimed in Claim 1 wherein the bistable stage comprises a third logic element which is responsive to the measurement signal, the reference signal, and the delayed reference signal to produce a setting signal, a fourth logic element which is responsive to the measurement signal and the delayed reference signal to produce a resetting signal, and a bistable trigger circuit having a setting input to which the setting signal is applied, a trigger input to which the resetting signal is applied, and a data input to which the second binary value is applied.

3. A phase detector substantially as herein described with reference to the accompanying drawings.

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Fig.1

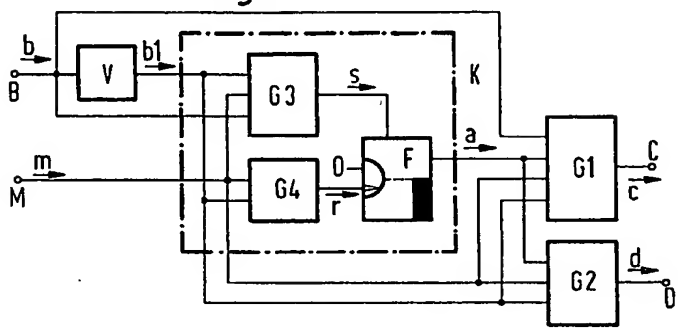
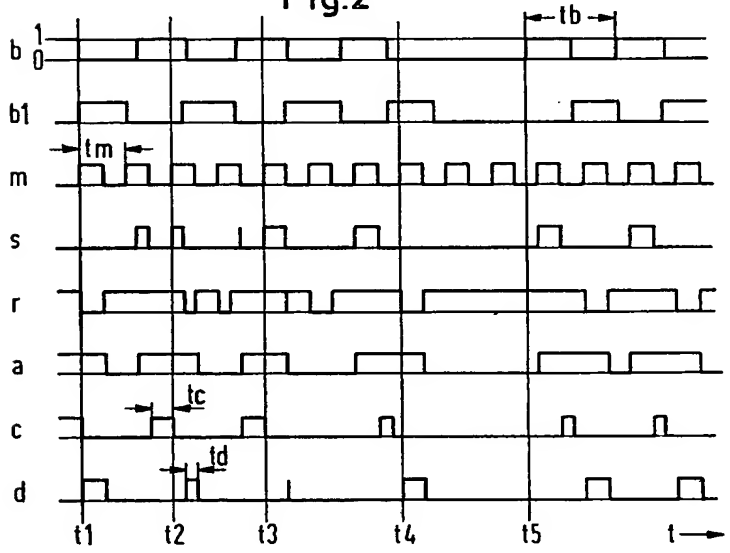


Fig.2



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Sheet 2

Fig.4

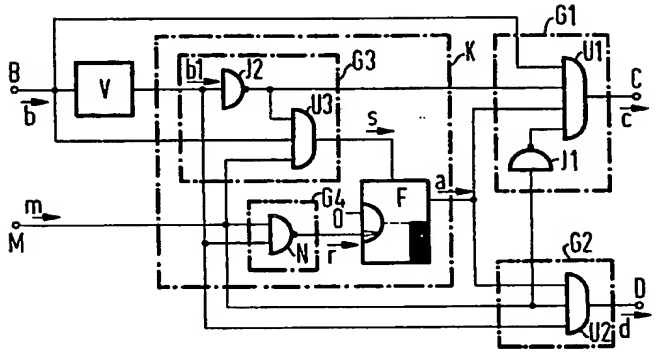

Fig.3